

In the Claims:

1. (Currently Amended) A method for fabricating fin field-effect transistors, comprising:
providing at least one original fin made of a single crystalline semiconductor material on a substrate by means of a first lithography step, then
providing a gate dielectric layer ~~on the~~ over longitudinal sides of the at least one original fin, then
providing a gate electrode layer made of a conductive gate electrode material ~~[[on]]~~ over the gate dielectric layer;
forming contact trenches that pattern the at least one original fin in a longitudinal direction by means of a second lithography step, wherein at least one transistor fin with a first head end and a second head end at a distance of a fin length from the ~~latter~~ first head end emerges from the at least one original fin, and wherein a gate electrode associated with the transistor fin emerges from the gate electrode layer; and then
processing the gate electrode, wherein the gate electrode recedes from both head ends;
and
forming a source/drain-region in each transistor fin from the respective two head ends respectively.
2. (Original) The method of claim 1, further comprising:
forming a source/drain region in the transistor fin from the two head ends; and
connecting the source/drain regions to source/drain contact structures made of a conductive contact material, wherein the gate electrode material recedes from both head ends except for a controllable channel length.

3. (Original) The method of claim 2, wherein, by means of the first lithography step, a plurality of original fins which are arranged next to one another and run parallel are formed and the gate electrode layer is prepatterned before the formation of the gate electrodes, and wherein the gate electrode layer in a bottom region of trenches formed between the original fins is subdivided into sections that are separated from one another and in each case associated with one of the original fins.

4. (Original) The method of claim 3, wherein the gate electrode layer essentially emerges from a conformal deposition, and wherein the pre patterning of the gate electrode layer comprises:
providing a nonconformal mask, by which at least the gate electrode material bearing on the original fin is covered, and at least the bottom region of the trenches is in each case left free;
and

removing sections of the gate electrode layer from the bottom regions not covered by the mask.

5. (Original) The method of claim 4, wherein the providing the nonconformal mask comprises:

depositing a nonconformal mask material, wherein the mask material is deposited with a smaller layer thickness in the bottom region of the trenches than on the original fins; and

causing the mask material to recede, so that the mask material is removed from the bottom region of the trenches and remains on the original fins.

6. (Original) The method of claim 5, wherein the nonconformal mask is removed after the pre patterning of the gate electrode layer.
7. (Original) The method of claim 2, wherein after the pre patterning of the gate electrode layer and before the second lithography step, a first isolating dielectric is applied to a pre patterned gate electrode layer.
8. (Original) The method of claim 2, wherein the contact trenches are introduced in the course of the second lithography step by means of a nonselective etching step.
9. (Original) The method of claim 2, wherein the process of causing the gate electrode to recede comprises an etching step which causes the gate electrode material to selectively recede.
10. (Original) The method as claimed in claim 9, wherein doped polysilicon is provided as gate electrode material.
11. (Original) The method of claim 10, wherein the gate electrode material is caused to recede by means of an etching step in a Cl plasma or an HBr plasma.
12. (Original) The method of claim 9, wherein divots produced as a result of the gate electrode material having been caused to recede are filled with a filling material.
13. (Original) The method of claim 2, wherein the source/drain regions are produced in the transistor fin by means of implantation.

14. (Original) The method of claim 3, wherein the contact trenches are lined at least partly by an isolating coating, wherein all of the conductive sections adjoining the respective contact trench are covered by means of the isolating coating, with the exception in each case of a source/drain region adjoining one of the contact trenches.

15. (Original) The method of claim 14, wherein the isolating coating is applied conformally and subsequently patterned on one side.

16. (Original) The method of claim 15,
wherein the etching resistance of the isolating coating is altered on one side by means of inclined implantation, and wherein an etching that is selective relative to altered and unaltered sections of the isolating coating is subsequently carried out.

17. (Original) The method of claim 2, wherein the contact trenches are filled with conductive material.

18. (Original) The method of claim 2, wherein a geometrical channel length of a channel region formed between the two source/drain regions is provided, such that the geometrical channel length is greater than or equal to a controllable channel length.

19-20. (Canceled)